ISSN 2229-5518

Efficient PID Controller Architecture for Autopilot based MAV Applications

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Abstract: In this paper implementation of digital PID controller using the concept of approximate adder for unmanned aerial vehicle is presented. Nowadays embedded control applications requires low power and fast acting PID controllers with a closed loop performance using less resources, resulting in cost reduction. In digital PID controller error signal is generated by using comparator which is analog in nature. By using ADC it is converted in to digital. There is no need to use ADC or DAC in ADPID. By using Approximate Arithmetic concept, the power consumption of the PID Controller is reduced inorder to increase flight time of MAV. The controller algorithm is synthesized, simulated using Cadence RTL Compiler mapped to TSMC 65 nm Technology Library. The results demonstrates that the proposed architectures are consuming low power than the conventional architecture.

Keywords PID Controller, MAV, Synthesis, Low Power

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1. Introduction

The development of PID (Proportional-Integral-Derivative) control theories has already 60 years so far, PID control has been one of the control system design method of the longest history. However, this method is still extensively used now [1, 2]. PID-controller and its modifications are the most common controllers in the industry. It is robust and simple to design, its operation is well known, it has a good noise tolerance, it is inexpensive and it is commercially available [2].

Implementation of digital PID controller has gone through several stages of evolution, from the early mechanical and pneumatic designs to the microprocessor based systems but these systems have the drawback of demanding control requirements of modern power conditioning systems will overload most of the microprocessors and the computing speed limits the use of microprocessor in complex algorithms.

2. Digital PID controller

To design an ADPID requires the knowledge to generate a proportional digital signal of the error, an integral digital signal for the errors over time, and a derivative digital signal for the change in error. These three separate signals need to be combined together to form a PWM control signal. An ADPID is mainly constructed by digital logic devices, such as 4-bit up/down counters, JK flip-flop, D flip-flop, multiplexer, and digital gates (*i.e*. AND, OR, EXOR…). In general, the error between the reference and encoded output is counted up or down by counters. The speed of counting depends on frequencies *fP*, *fI* and *fD*. Then, the summation of the counters is counted to zero at frequency *fA*. The control signal generated by an ADPID is in PWM form, and the corresponding direction is determined by the most significant bit of the adders.

It is totally frequency base method of PID control. The gain of the P, I, D term can be adjust by simply setting the appropriate frequency of the counter for the P, I, D term and the frequency of the final summation counter.
The gain of the Proportional K_P , integral K_I and derivatives K_D are define by using the frequency of the counters.

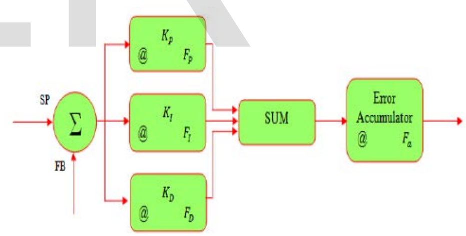


Fig 1: Block Diagram of ADPID

$$K_P = \frac{f_P}{f_A} \quad ....(2)$$

$$K_I = \frac{f_I}{f_A} \quad ....(3)$$

$$K_D = \frac{f_D}{f_A} \quad ...(4)$$

The base frequency, *fA*, is the counting frequency for the combined counters. It is directly related to *fP*, *fI* and *fD*. It can be determined after any one of the proportional, integral or derivative frequencies is known. Technically, low frequencies cause inaccurate counting, whereas extremely high counting frequencies create problems such as integrator windup. As a result, more hardware is needed to prevent counting overflow. Hence it is crucial to design a proper counting frequency, to obtain an accurate model yet reduce the hardware to the minimum.

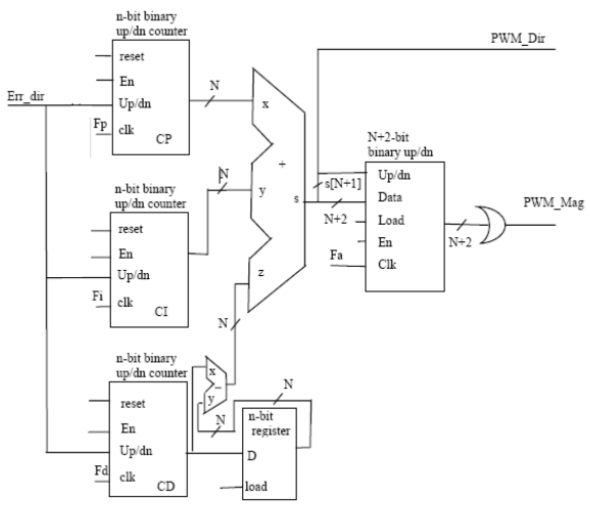


Figure 2: Basic structure of ADPID

3. PID controller for unmanned aerial vehicle

Unmanned aerial vehicle is remotely piloted or self-piloted (without pilot) aircraft which can carry many different types of accessories such as cameras. In many types of UAV's servo motors are using for adjusting movements, sensors and communications equipment. Control of the movements and flying systems in the UAV is customarily done by using the microcontroller's optimal controllers or conventional PID control techniques. The main objective of the work reported in this paper is to evaluate the performance of each of existing and proposed approximate PID controllers separately and will show the characteristics of the each of proposed PID and existing controllers, and which controller is better for obtaining the desired response.

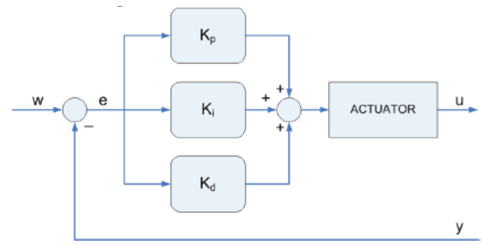
In [13] an attempted is made to determine the optimal coefficients of PID controller that can reject disturbances and still operate the MAV in stable positions. Basic PID controller is designed and is adopted to control the MAV, a modified techniques incorporating ISA-PID is designed to reject disturbances.The pid structure is defined by the equation

$$G_{PID}(s)=K_p e(t)+K_d\frac{de(t)}{dt}+K_i\int_0^t e(\tau)d(\tau)+K_p\left[1+\frac{1}{T_i s}+\frac{T_d s}{\frac{T_d s}{N}+1}\right]$$

Where *Kp*/*Ti* = *Ki*, , *Kp* * *Td* = *Kd*, and *N* = filter constant.

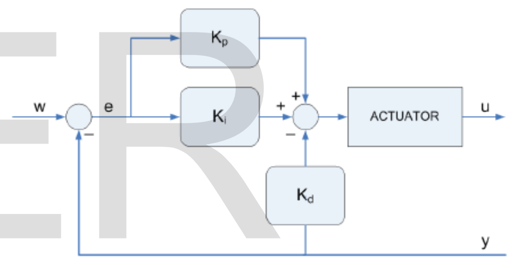
In control theory the ideal PID controller in parallel structure is represented in the continuous time domain as in equation

$$u(t)=K_p e(t)+K_i\int_0^t e(\tau)d\tau+K_d\frac{de(t)}{dt}$$

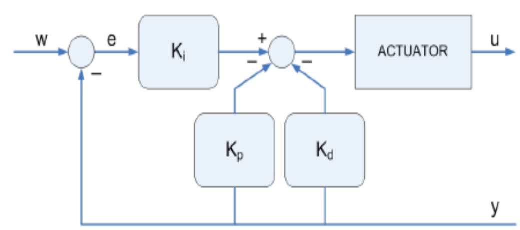


Block diagram of ideal PID controller

The problem with conventional PID controllers is their reaction to a step change in the input signal which produces an impulse function in the controller action. There are two sources of the violent controller reaction, the proportional term and derivative term. There are two PID controller structures which avoid this issue



Block diagram of type B pid controller



Block diagram of type C pid controller

Therefore for any given pid structure the approximation arithmetic can be used as the arithmetic components are applied for all pid controllers.

Approximate Arithmetic: In most of the control systems there exists marginal room for error. The approximation can be applied to the control system without impacting its normal operation. State of the art approximation techniques used are Truncation, Rounding etc. But existing

ISSN 2229-5518

approximation techniques impact control system operation & result in error.

In MAV applications, we can use approximation to reduce the system complexities. Based upon the approximate arithmetic datapath components, we can achieve low power consumption of the Controller which will increase the Flight Time of the MAV.

4. Full Adder

A full **adder** adds binary numbers and accounts for values carried in as well as out. For example, a one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and C_{in}; *A* and *B* are the operands, and C_{in} is a bit carried in from the previous less-significant stage and provides sum and carry outputs.

Existing Full adder:

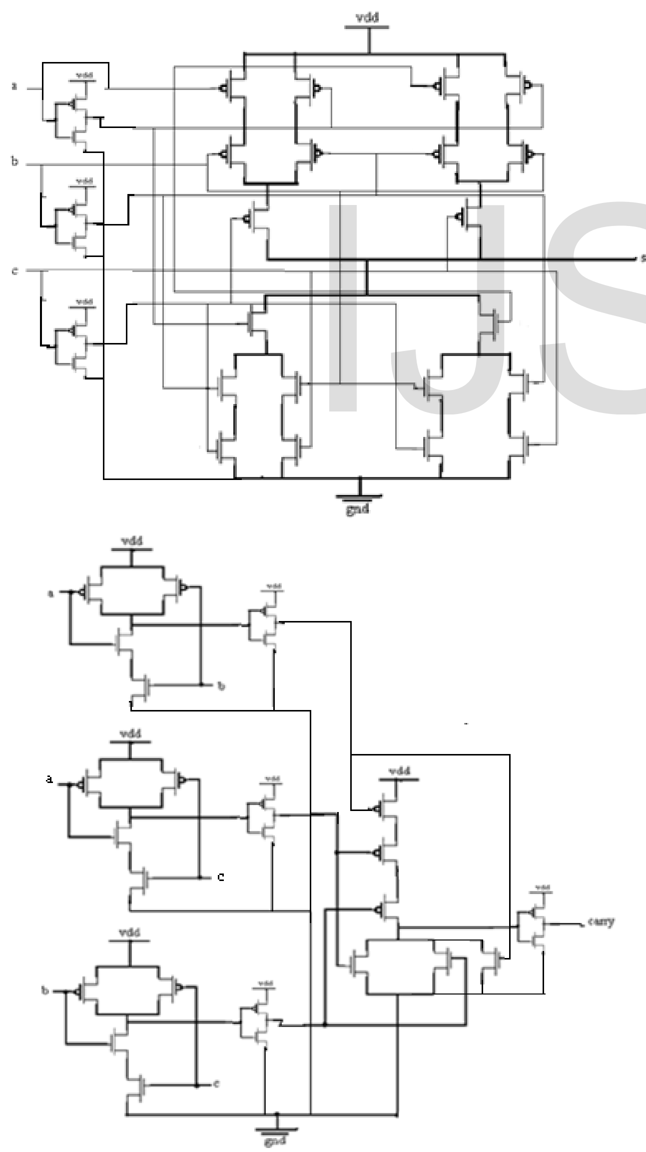


Fig 3: Existing Full Adder

Proposed Fulladder:

In the proposed approximate based full adder, the carry path is approximated inorder to reduce power. In the proposed approximate based Full Adder architecture, the sum path of the full adder is one 3-input XOR and carry path is approximated to two AND gates and one OR gate as shown in fig below. This will result in both area & power reduction.

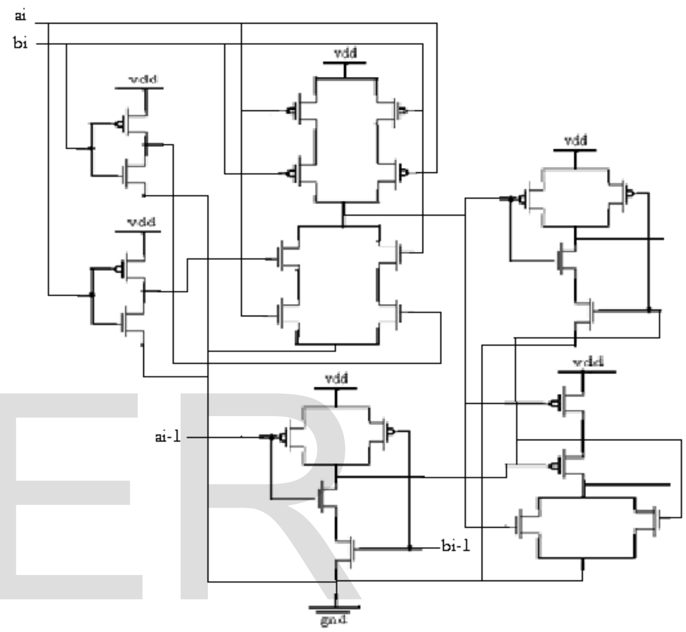


Fig 4: Proposed Approximate Full Adder

5. Results and discussions:

Releasing the stringent accuracy requirement would potentially offer greater freedom to create a design with better performance or energy efficiency. As the number of gates are reduced in approximate adder there will less power consumption and area will less when compared to the existing full adder.

The digital PID controller with conventional and proposed architectures was modeled using Verilog HDL and both the architecture's functionality has been verified using model-sim simulator. Both the designs were synthesized with standard ASIC methodology using Cadence RTL compiler by targeting the CMOS 65nm technological node. Proposed low power concept was applied to all possible parts of the digital PID architecture and the importance of datapath architectural optimizations are observed. The results of the conventional and proposed architectures are tabulated in Table I.

	Existing	Approximate	% Change
Area(cells area)	918	897	0.02
Delay(ns)	1328	1964	+47.7
Dynamic Power(nW)	25814.884	19118.124	26
Leakage Power(nW)	5646.692	5225.618	7.4
Total Power(nW)	31461.577	24343.742	22.38

Table I: Parameter comparison proposed 8 bit ADPID

6. Conclusion:

This paper presented a methodology to design PID controllers using approximate adders for unmanned aerial vehicle. Two design scenarios have been evaluated: one is the conventional design scenario in which existing full adder is used and second one use of proposed approximate full adder. In the proposed full adder accuracy is sacrificed for better performance was power consumption and area is reduced. The performance enhancement were seen

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